



SSC8121GN5

P-Channel Enhancement Mode MOSFET

➤ Features

VDS	VGS	RDSON Typ.	ID
-20V	±8V	140mR@-4V5	-3A
		190mR@-2V5	
		280mR@-1V8	

➤ Description

This device is produced with high cell density DMOS trench technology, which is especially used to minimize on-state resistance. This device particularly suits low voltage applications such as portable equipment, power management and ther battery powered circuits, and low in-line power dissipation are needed in a very small outline surface mount package.

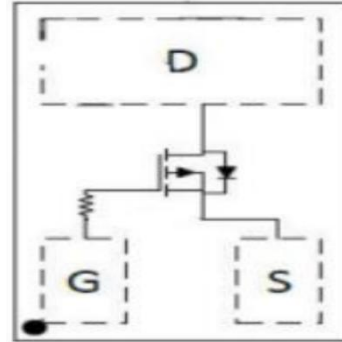
➤ Applications

- Load Switch
- Portable Devices
- DCDC conversion

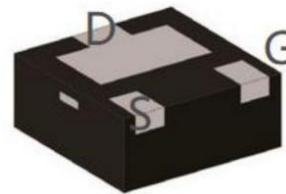
➤ Ordering Information

Device	Package	Shipping
SSC8121GN5	DFN1616	3000/Reel

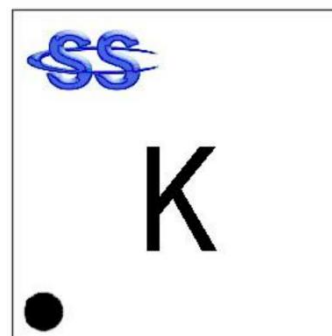
➤ Pin configuration



Top view



DFN1616



Marking



➤ **Absolute Maximum Ratings**($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-to-Source Voltage	-20	V
V_{GSS}	Gate-to-Source Voltage	± 8	V
I_D	Continuous Drain Current ^a	-3	A
I_{DM}	Pulsed Drain Current ^b	-12	A
P_D	Power Dissipation ^c	2	W
T_J	Operation junction temperature	-55 to 150	$^{\circ}\text{C}$
T_{STG}	Storage temperature range	-55 to 150	$^{\circ}\text{C}$

➤ **Thermal Resistance Ratings**($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Maximum	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance ^a	58	$^{\circ}\text{C}/\text{W}$

Note:

- The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz.copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The value in any given application depends on the user is specific board design. The current rating is based on the $t \leq 10\text{s}$ thermal resistance rating.
- Repetitive rating, pulse width limited by junction temperature.
- The power dissipation P_D is based on $T_J(\text{MAX})=150^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

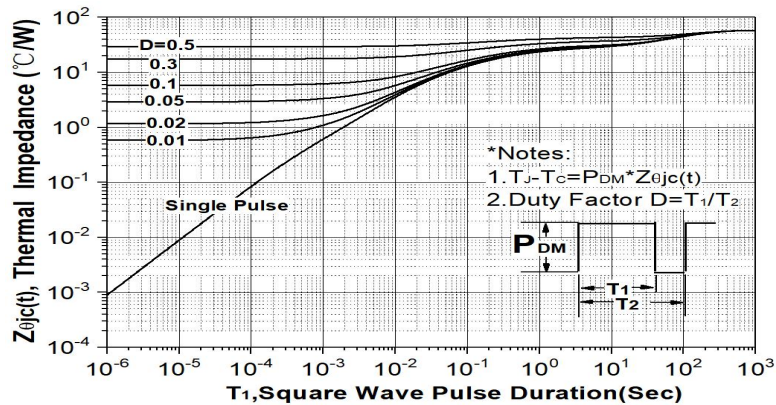
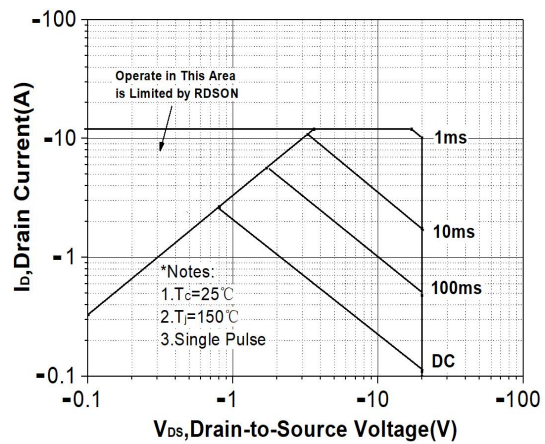
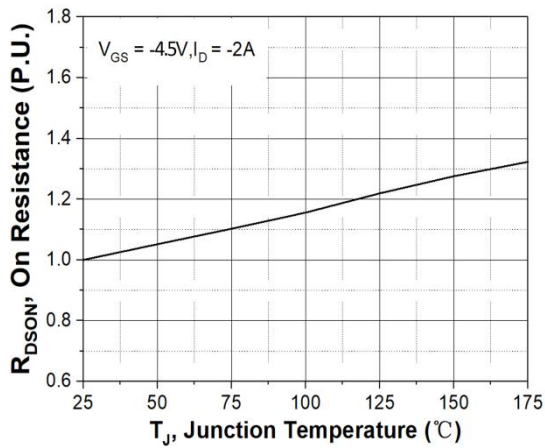
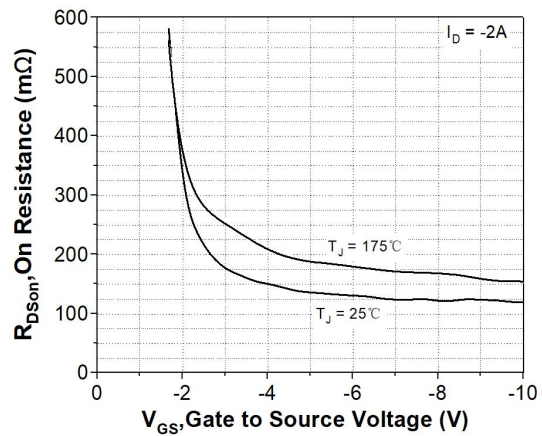
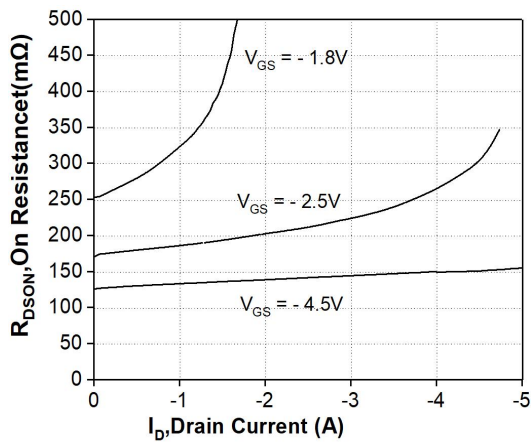
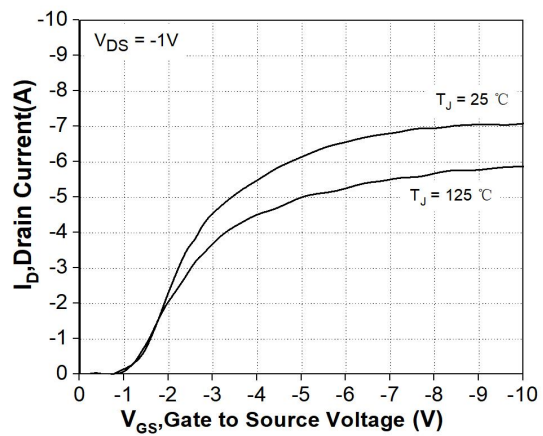
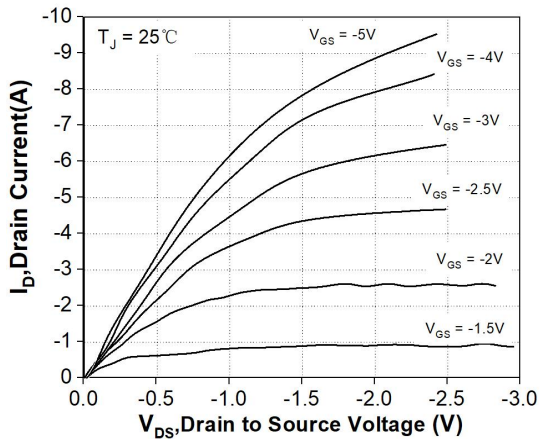


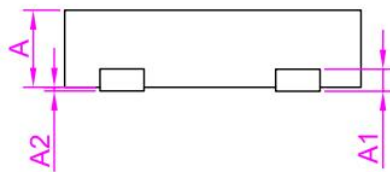
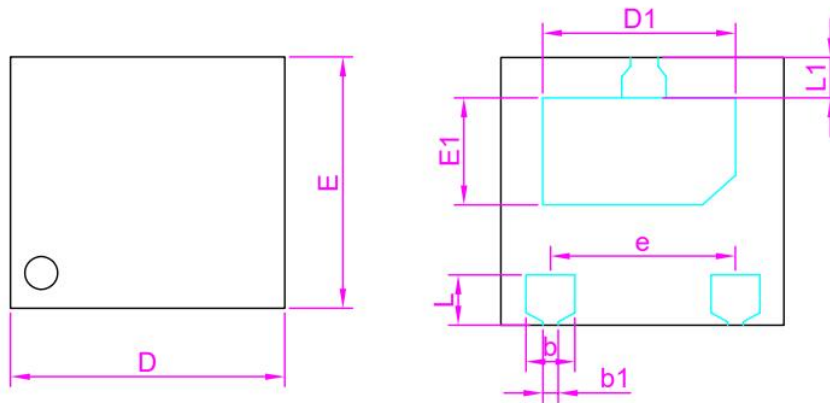
➤ **Electronics Characteristics**($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-20			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.45	-0.7	-1.5	V
$R_{DS(on)}$	Drain-Source On-Resistance	$V_{GS}=-4.5V, I_D=-0.45A$		140	350	mR
		$V_{GS}=-2.5V, I_D=-0.35A$		190	450	
		$V_{GS}=-1.8V, I_D=-0.25A$		280	700	
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-20V, V_{GS}=0V$			-1	μA
I_{GSS}	Gate-Source leak current	$V_{GS}=\pm 8V, V_{DS}=0V$			± 100	nA
G_{FS}	Transconductance	$V_{DS}=5V, I_D=-2A$		6.5		S
V_{SD}	Forward Voltage	$V_{GS}=0V, I_S=-1A$		-0.8	-1.3	V
C_{iss}	Input Capacitance	$V_{DS}=-10V, V_{GS}=0V, f=1MHz$		214		pF
C_{oss}	Output Capacitance			112		
C_{rss}	Reverse Capacitance			38		
$T_{D(ON)}$	Turn-on delay time	$V_{GS}=-4.5V,$ $V_{DS}=-10V, R_L=5R$ $R_G=3R$		12		ns
T_r	Rise time			6		
$T_{D(OFF)}$	Turn-off delay time			25		
T_f	Fall time			10		
Q_g	Total Gate charge	$V_{GS}=-4.5V, V_{DS}=-10V$ $I_D=-2A$		3.5		nC
Q_{gs}	Gate Source charge			0.5		
Q_{gd}	Gate Drain charge			1.2		



➤ Typical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)



➤ Package Information


COMMON DIMENSION (MM)			
PKG	DFN1616-3L		
REF.	MIN.	NOM.	MAX.
A	0.50	0.55	0.60
D	1.55	1.60	1.65
E	1.55	1.60	1.65
b	0.35	0.40	0.45
L	0.35	0.40	0.45
e	1.00BSC		
D1	1.15	1.20	1.25
E1	0.50	0.55	0.65
b1	0.15	0.20	0.25
L1	0.20	0.25	0.30
A1	0.15BSC		
A2	0.00	0.025	0.05



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